REMARKS

Applicants respectfully traverse and request reconsideration. Claims 1, 2, 4, 6-10, 12-16 and 18-21 are pending. Claim 22 is new.

Claims 1, 2, 4, 6-10, 12-16, and 18-21 stand rejected under 35 U.S.C. § 112, 2d paragraph, as allegedly indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Claims 1, 2, 4, 7, 10, 12, 13, and 14 have been amended accordingly.

The amendments to Claims 7, 10, 12, and 13 correct typographical errors and do not narrow the scope of the claims as originally filed.

As to Claim 14, the Office Action states that "The control signal" by itself cannot distinguish voltage levels of reference and input signals. However, Claim 7 recites "providing either of at least an I/O pad supply voltage or a reference supply voltage for a single gate oxide differential receiver based on a control signal.

Applicants wish to thank the Examiner for the indication that Claims 6-7, 9, 19, 12, 13, 15, 16, 20 and 21 would be allowable if rewritten in independent form.

CLAIM REJECTED UNDER 35 U.S.C. § 102(E)

Claim 1 stands rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,091,300 (Setty). Setty discloses a differential comparator circuit commonly used in high-speed analog to digital (A/D) converters. (Setty Col. 4, lines 26-29). Before amplification, Setty requires the differential amplifier enter into an "auto-zero" mode in order to compensate for any output offset.

> Referring to FIG. 2, **before differential amplifier 10 begins amplification**, switches S1 and S2 are closed and the inputs V_{IP} and V_{IM} are set at their common-mode voltage V_{CM}. Nodes V1 and V2 **charge to a common-mode voltage set by the output of differential amplifier** 10. In an offset-free differential amplifier, the voltages at nodes V1 and V2 are substantially equal to the output common-mode voltage of the differential amplifier. However, in the presence of the amplifier offset, the difference between the voltages on nodes V1 and V2 is substantially equal to

> the amplifier offset. This mode, where the offset and input common-mode of the amplifier and the reference common mode of the input signal are acquired and/or set, is commonly referred to as the "**auto-zero**" or "offset acquisition" mode.

(Setty, Col. 1, lines 41-54). Accordingly, Setty requires entry into an auto-zero mode before differential amplifier begins amplification.

SETTY AS CITED FAILS TO RECITE "AT LEAST ONE OF THE SELECTED RECEIVER SUPPLY VOLTAGES IS HIGHER THAN A MAXIMUM VOLTAGE LEVEL OF THE INPUT VOLTAGE"

Firstly, Setty teaches against "at least one of the selected receiver supply voltages is higher than a maximum voltage level of the input voltage" because Setty teaches that the supply voltage is dropped as a result of entering the "auto-zero" mode before differential amplifier begins amplification.

> Assuming that the differential amplifier is configured as shown in FIG. 2 (with differential amplifier 20 replacing differential amplifier 10), **during the auto-zero mode** when switches S1 and S2 are closed, the output common-mode voltage of the differential amplifier 20 is changed by **dropping the supply voltage** thereto by a predetermined amount. This is symbolically shown by inserting a battery V.sub.A between the external supply voltage V.sub.DD and the sources of devices M5 and M6 as shown in FIG. 3. With this modification, during the auto-zero mode, the voltages at nodes V1 and V2 are equal to V.sub.DD -V.sub.A |.V.sub.GS|., where .|.V.sub.GS|.. is the absolute value of the gate-source voltage of transistors M5 and M6.

(Setty, Col. 3, lines 4-16). Since Setty drops the supply voltage during the auto-zero mode, and the auto-zero mode is entered before amplification begins, Setty teaches an approach completely different from "at least one of the selected receiver supply voltages is higher than a maximum voltage level of the input voltage." Secondly, Setty is silent with respect to lowering the supply voltage based on any input voltage because Setty teaches an opposite approach, rather the dropping of the supply voltage for the "auto-zero" mode. As a result, Setty fails to teach all the elements as arranged in claim 1. For any or all of the above reasons, Claim 1 is allowable.

As to Claim 2, since Setty, as understood, does not "select[s] the differential receiver supply voltage that is a higher voltage than the I/O pad supply voltage." According to the Office

Action on page 4, reference # 4, the input/output pad supply voltage corresponds to Vdd EXTERNAL terminal of Figure 3 in Setty. However, since Vdd INTERNAL is always less than Vdd EXTERNAL, Setty fails to teach, and teaches an approach opposite to "select[s] the differential receiver supply voltage that is a higher voltage than the I/O pad supply voltage." Accordingly, for at least this reason, claim 2 is allowable.

CLAIM REJECTION UNDER 35 U.S.C. § 103(A)

Claims 4, 8, 10 and 18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Setty. Firstly, Applicants respectfully reassert the relevant remarks made above with respect to Claim 1.

SETTY AT LEAST FAILS TO TEACH "WHEREIN THE SWITCHABLE VOLTAGE SUPPLY CIRCUIT SELECTS THE DIFFERENTIAL RECEIVER SUPPLY VOLTAGE FOR THE SINGLE GATE OXIDE DIFFERENTIAL RECEIVER TO BE A VOLTAGE LEVEL HIGHER THAN A MAXIMUM VOLTAGE LEVEL OF THE INPUT LINE.

As to claim 4, Setty at least fails to teach "wherein the switchable voltage supply circuit selects the differential receiver supply voltage for the single gate oxide differential receiver to be a voltage level higher than a maximum voltage level of the input line." By contrast, Setty teaches:

Secondly, rather than select the supply voltage based on "a maximum voltage level of the input line" as claimed, Setty, reacts when entering into "auto-zero" mode. Accordingly, Setty does not teach all the elements as arranged in the claim.

Thirdly, the Office Action acknowledges that Setty does not disclose a reference voltage on a first differential input and an input voltage on a second differential input. However, Setty teaches against "receives a reference voltage on a first differential input and an input voltage on a second differential input" because Setty teaches the incompatible approach of causing switches S1 and S2 to close causing the inputs V_{IP} and V_{IM} to be set at their common-mode voltage V_{CM}. Setty requires that the circuit enter an "auto-zero" mode where switches S1 and S2 are closed causing the inputs V_{IP} and V_{IM} to be set at their common-mode voltage V_{CM}. Since Setty requires that inputs V_{IP} and V_{IM} be set at their common-mode voltage V_{CM}, Setty teaches against,

"a reference voltage on a first differential input and an input voltage on a second differential input."

Fourthly, rather than select the supply voltage as claimed, "to be a voltage level higher than a maximum voltage level of the input voltage", Setty merely sets the inputs to their common-mode voltage. Accordingly, Setty does not teach "wherein the switchable voltage supply circuit selects the differential receiver supply voltage for the single gate oxide differential receiver to be a voltage level higher than a maximum voltage level of the input line."

Fiftly, Setty teaches against the claimed invention because the modifications suggested would change the principle of operation, i.e., (A/D converter). Setty's circuit would not function as an A/D circuit because as an input/output pad the outputs Vom and Vop driven by M5 and M6 do not provide the appropriate range swing, i.e. negative or positive wing. For example, when the input signal at VIP and VIM is at a voltage corresponding to a logic 0, M1 and M2 would switch off thus preventing outputs VOM and VOP from providing a proper voltage corresponding to a logic level. Also, the single gate oxide gate of the claims can withstand the selected supply voltages, whereas the circuit in Setty would fail because the gate to source and gate to drain maximum limits would be exceeded.

Claim 8 requires that the receiver of Claim 1 "generate an output signal to circuitry for a videographics processor." Hence, an output signal must be generated as well as suitable coupling to communicate the output signal to the circuitry for a videographics processor. Setty is silent as to any such structure.

As to Claim 10, Applicants respectfully reassert at least the relevant remarks made above with respect to Claims 1 and 4.

As to Claim 18, Applicants respectfully reassert the relevant remarks made above with respect to Claim 1 and further note that Setty fails to recite an isolation output buffer as recited in the claim. Accordingly, this claim is also believed to be in condition for allowance.

Attached hereto is a marked up version of the changes made to the claims by the current amendment. The attached page is captioned "Version With Markings to Show Changes Made."

Applicants respectfully submit that the claims are in condition for allowance and respectfully request that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Once Amended) An integrated differential receiver for an input/output pad comprising:

a single gate oxide differential receiver that receives an input voltage; and

a switchable voltage supply circuit operatively coupled to the single gate oxide differential receiver, switchable through at least one control signal to select [a] at least one differential receiver supply voltage for the single gate oxide differential receiver wherein at least one of the selected receiver supply voltages is [different from the input/output pad supply voltage] higher than a maximum voltage level of the input voltage.

2. (Once Amended) The receiver of claim 1 wherein the switchable voltage supply circuit is coupled to an input/output pad supply voltage and selects the differential receiver supply voltage that is a higher voltage than the I/O pad supply voltage.

4. (Once Amended) The receiver of claim 1 wherein the differential receiver receives a first reference voltage on a first differential input and [an] the input voltage on a second differential input and wherein the switchable voltage supply circuit selects the differential receiver supply voltage for the single gate oxide differential receiver to be a voltage level higher than [a] the maximum voltage level of the input voltage.

7. The receiver of claim 1 wherein the single gate oxide differential receiver includes a transistor operatively coupled to an input transistor of a single gate differential input stage having a gate coupled to [the] a first reference voltage, a source coupled to the single gate oxide differential receiver supply voltage, a drain coupled to a drain of the input transistor that receives the input signal.

10. An integrated differential receiver for an input/output pad comprising:

a single gate oxide differential receiver that receives a first reference voltage on a first differential input and an input voltage on a second differential input;

a switchable voltage supply circuit operatively coupled to the single gate oxide differential receiver, switchable through at least one control signal to select a differential receiver supply voltage for the single gate oxide differential receiver wherein at least one of the selected receiver supply voltages is a voltage level higher than a maximum voltage level of the input voltage; and

an isolation output buffer operatively coupled to an output of the differential receiver and to core logic.

12. The receiver of claim [11] 10 wherein the switchable voltage supply circuit is operatively responsive to at least two control signals.

13. The receiver of claim [11] 10 wherein the single gate oxide differential receiver includes [the single gate oxide differential receiver includes] a transistor, operatively coupled to an input transistor of a single gate differential input stage having a gate coupled to [the] a first reference voltage, a source coupled to the single gate oxide differential receiver supply voltage, a drain coupled to a drain of the input transistor that receives the input signal.

14. A method for controlling a voltage supply for a differential receiver comprising the steps of:

providing either of at least an I/O pad supply voltage [and] or a [second] reference supply voltage for a single gate oxide differential receiver based on a control signal such that the reference supply voltage is selected as the differential receiver supply voltage when the control signal indicates a maximum input signal voltage to be less than the [second] reference supply voltage; and

providing the I/O pad supply voltage as the differential receiver supply voltage when the control signal indicates [a] the maximum input signal voltage to be greater than the [second] referenced supply voltage.